Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

Claims 1-27 are withdrawn.

28. (New) A processor, comprising:
multiple programmable engines integrated within the processor; and
circuitry integrated within the processor to map resources within the multiple engines into a single address space.

29. (New) The processor of claim 28, wherein the resources within the multiple programmable engines comprise registers within the multiple programmable engines.

30. (New) The processor of claim 28, wherein the single address space comprises addresses corresponding to shared resources external to the multiple programmable engines.

31. (New)The processor of claim 30, wherein the shared resources external to the multiple programmable engines comprise at least one of: a memory internal to the processor, a randomly accessible memory external to the processor, and a Peripheral Component Interconnect (PCI) unit.

32. (New) The processor of claim 28, wherein the multiple programmable engines comprise multiple programmable multi-threaded engines.

33. (New) The processor of claim 28, further comprising an interface to a media access controller (MAC).

34. (New) The processor of claim 28, wherein the circuitry comprises circuitry to receive a command from a programmable processor other than the multiple programmable engines.

35. (New) The semiconductor chip of claim 34, wherein the programmable processor other than the multiple programmable engines comprises a programmable processor integrated within the processor.

36. (New) A method, comprising:

mapping an address in a single address space to a resource within one of a set of multiple programmable engines integrated within a processor, the single address space including addresses for different ones of the resources in different ones of the multiple programmable engines.

37. (New) The method of claim 36, further comprising receiving a command specifying the address in the single address space.

38. (New) The method of claim 37, wherein the command comprises one of: a read command and a write command.

39. (New) The method of claim 37, wherein the receiving the command comprises receiving the command from a programmable processor other than one of the multiple programmable engines.

40. (New) The method of claim 39, wherein the programmable processor comprises a programmable processor integrated within the processor.

41. (New) The method of claim 36, wherein the resource within the one of the set of multiple programmable engines comprises at least one register.

42. (New) The method of claim 36, wherein the single address space comprises addresses corresponding to shared resources external to the multiple programmable engines

43. (New) The method of claim 36, wherein the multiple programmable engines comprise multiple programmable multi-threaded engines.

44. (New) A device, comprising:

at least one Ethernet media access controller (MAC); and

at least one processor coupled to the at least one Ethernet media access controller, the processor comprising:

multiple programmable multi-threaded engines; and

circuitry to map resources within the multiple engines and resources external to the multiple engines into a single address space, the resources within the multiple engines comprising registers, the resources external to the multiple engines comprising at least one Random Access Memory (RAM) external to the processor.

45. (New) The device of claim 44, wherein the processor further comprises a programmable processor integrated within the processor, the programmable processor having a different architecture than the multiple engines.